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Intellectual Property Group
2700 First Indiana Plaza
135 North Pennsylvania Street
Indianapolis, Indiana 46204
(317) 684-5000

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PATENT APPLICATION jc954 U.S. PTO

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

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Sir:

Transmitted herewith for filing under 35 U.S.C. 1.111 and 37 C.F.R. 1.53 is the patent application of:

Applicants: Jochen Stinus and Monika Banzhaf

Title: PROGRAMMABLE FIELD DEVICE

Atty. Docket No.: 9092-0138

Certificate Under 37 C.F.R. 1.10

Express Mail Label No.: EL591985575US

Date of Deposit: October 16, 2000

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Sherron E. Walker
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Sherron E. Walker
Signature of Person Mailing Paper or Fee

09/688681 10/16/00

Enclosed are:

- X Specification (20 pages)
- X Claims (26 claims)
- X Drawings (4 sheets)
- X Abstract
- X Declaration and Power of Attorney
- ____ An assignment of the invention to ____
- X Check to cover the total fees for filing this application as calculated below
- ____ Recordation Form Cover Sheet
- ____ Check to cover $40 fee for recording assignment
- X Claim of Priority
- X Priority Document
- ____ Information Disclosure Statement
- ____ Form PTO-1449
- ____ Copies of ____ Cited References
- X Preliminary Amendment

CLAIMS AS FILED					
	NUMBER FILED		NUMBER EXTRA	RATE	FEE
BASIC FEE (37 C.F.R. 1.16 (a))				$710	$710
TOTAL CLAIMS (37 C.F.R. 1.16(c))	26	- 20 =	6	$18	$108
INDEPENDENT CLAIMS (37 CFR 1.16(b))	3	- 3 =	0	$80	$0
MULTIPLE DEPENDENT CLAIM PRESENT	(37 C.F.R. 1.16(d))			$270	
* NUMBER EXTRA MUST BE ZERO OR LARGER				TOTAL	$818
If applicant has small entity status under 37 C F R 1.9 and 1.27, then divide total fee by 2, and enter amount here.				SMALL ENTITY TOTAL	NO

FEE FOR RECORDING ASSIGNMENT ____

TOTAL FEES $818.00

The Commissioner is hereby authorized to charge any additional filing fees under 37 C.F.R. 1.16 or processing fees under 37 C.F.R. 1.17 which may be required, or credit any overpayment, to Bose McKinney & Evans LLP's Deposit Account No. 02-3223. A duplicate copy of this sheet is enclosed.

CORRESPONDENCE ADDRESS:
Intellectual Property Group
Bose McKinney & Evans LLP
2700 First Indiana Plaza
135 North Pennsylvania Street
Indianapolis, Indiana 46204

303282

Attorney of Record
Printed Name: James A. Coles
Registration No.: 28,291
Daytime Phone No.: (317) 684-5000

Date: October 16, 2000

BOSE McKINNEY & EVANS LLP

2700 First Indiana Plaza
135 North Pennsylvania Street
Indianapolis, Indiana 46204

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group:	Unknown
Atty. Docket:	9092-0138
Applicants:	Stinus et al.
Title:	PROGRAMMABLE FIELD DEVICE
Serial No.:	Unknown
Filed:	Herewith
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Sherron E. Walker
Signature of Person Mailing Paper or Fee

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Preliminary to the examination of the above-identified patent application submitted herewith, applicant respectfully requests entry of the following amendment.

IN THE CLAIMS

Please amend claim 16 as follows:

16. (Amended) The device of claim 12 [and 15], wherein the control circuit is further configured to provide the microprocessor read access to the memory area containing the second program[m] code for executing said program code.

Please add the following new claim:

--26. The device of claim 15, wherein the control circuit is further configured to provide the microprocessor read access to the memory area containing the second program code for executing said program code.--

REMARKS

With the entry of the foregoing amendment, the application is believed to be in condition for allowance. Consideration of the claims leading to their allowance and passage of the application to issuance is respectfully requested.

Respectfully submitted,

BOSE McKINNEY & EVANS LLP

James A. Coles
Reg. No. 28,291

JAC/sw
(317) 684-5251
Indianapolis, Indiana

303257

Programmable Field Mounted Device

Field of the Invention

This invention relates to a programmable field mounted device with field mounted device electronics and to a method of reconfiguring the latter.

Background and Summary of the Invention

In process automation technology, analog or digital measurement signals representative of process variables are preferably generated using field mounted devices. The process variables may represent, for example, mass flow rate, tank contents level, pressure, temperature, etc., which are sensed with suitable sensors.

Such field mounted devices are commonly connected with one another and with associated process control computers via a suitable data transmission system, to which they send measurement signals via, e.g., a 4- to 20-mA current loop and/or via a digital data bus. For the data transmission systems, field bus systems, particularly serial systems, such as Profibus-PA, Foundation Fieldbus, CANbus, etc. and the corresponding communications protocols are used.

By means of the process control computers, the transmitted measurement signals are processed and visualized as corresponding measurement results, e.g., on monitors,

and/or converted to control signals for actuators, such as solenoid valves, electric motors, etc.

Besides their primary function, namely to generate measurement signals, present-day field mounted devices have various additional functionalities which support an efficient and reliable control of the process to be monitored. These include such functions as self-checking by the field mounted device, storing measured values, generating control signals for actuators, etc. Because of this high functionality of the field mounted devices, process-controlling functions can be shifted increasingly to the field level, so that process control systems can be organized as correspondingly decentralized systems. These additional functionalities also relate, for example, to the start-up of the field mounted device and to its connection to the data transmission system.

These and further functions of field mounted devices are commonly implemented using field mounted device electronics, which comprise a microcomputer and suitable software that is part of the microcomputer. The software is programmed into a permanent storage, such as a PROM, or a nonvolatile, persistent storage, e.g., an EEPROM, of the microcomputer prior to or during the start-up of the field mounted device, and, for the operation of the field mounted device, can be loaded into a volatile storage, such as a RAM.

The processes monitored by the field mounted devices are subject to constant modification both with respect to the construction of the plants and with respect to the time

sequences of individual process steps. Accordingly, the field mounted devices must be adapted to changing process conditions and further developed. This applies to the sensors, but particularly also to the implemented functions, such as the control of the sensor, the processing of the measurement signals, or the presentation of the measurement results, and to the communication with the data transmission system.

For such reconfigurations of the functions implemented in the field mounted device electronics, mainly corresponding modifications of the stored software are necessary in programmable field mounted devices. Such reconfigurations are commonly made in situ via a control unit connected to the field mounted device, and may comprise, for example, changes to individual instrument parameters or the loading of complete processing programs.

One way of implementing the reconfigurations is to replace the storages containing software to be modified by storages containing the modified software, which can be done, for example, by rearranging individual storage elements or replacing the respective memory boards. This necessitates opening the housing of the field mounted device, so that the latter must be switched off.

Another disadvantage is that during such a reconfiguration, the affected plant sections also may have to be shut down.

If nonvolatile storage devices are used for storing the software, another possibility of reconfiguring the field mounted device electronics is to download the modified

software from a mass storage, e.g., a diskette, a CD-ROM, or a magnetic tape, via a download bus into a volatile storage of the signal processing unit, e.g., into a RAM. The software to be modified can then be erased in the nonvolatile storage and be replaced by the software contained in the volatile storage.

For these reconfigurations, the housing of the field mounted device need not be opened; however, the field mounted device must be switched off-line, i.e., it must be put out of operation. This reduces the reconfiguration time considerably, but a shutdown of affected plant sections cannot be ruled out.

Another disadvantage of such a reconfiguration is that the software to be modified is no longer loaded while the modified software has not been completely loaded yet. The longer this condition lasts, the higher the probability that external disturbances, such as power supply variations, will occur. Because of the relatively high power requirement for writing to nonvolatile storages and because of the generally small energy reserves in field mounted devices, particularly in fail-safe devices, this may result in the software to be loaded being erased from the volatile storage and thus being not available for the reconfiguration. Accordingly, the reconfiguration will terminate uncompleted. This erroneous condition can be overcome, for example, by resetting the microcomputer to preprogrammed default settings and reloading the software, but this prolongs the downtime of the field mounted device and possibly of the affected plant section.

In many cases, however, a reduction of error probability by increasing the available electric power using, for example, additional, energy-storing accumulator and/or capacitance networks conflicts with the demand for field mounted device electronics with minimum space and power requirements and with minimum circuit complexity. Furthermore, for many applications, particularly in hazardous areas, the storage capacity of energy storage circuits is limited by relevant standards to a maximum energy reserve.

It is therefore an object of the invention to provide a programmable field mounted device, particularly an intrinsically safe field mounted device, comprising field mounted device electronics which are reconfigurable during on-line operation and which during and after the reconfiguration are not placed in an undefined or erroneous state caused by this reconfiguration. Furthermore, at least the last executed software is to be stored in the field mounted device electronics even after a power failure during reconfiguration.

To attain this object, the invention consists in a method for configuring a field mounted device having a memory, the method comprising the steps of:

running a computational process having data read access to an activated first memory area storing a programmable first device configuration;

deactivating the first memory area, wherein said step comprises precluding said computational process to access the first memory area; and

activating a deactivated second memory area storing a programmable second device configuration, wherein said step

comprises granting said computational process data read access to the second memory area.

Prefered embodiments and developments of the method of the invention are defined by the respective subclaims.

Furthermore, the invention consists in a programmable field mounted device, comprising:

a memory circuit including a plurality of memory areas, each memory area storing program codes, each memory area selectively activated;

a control circuit configured to generate a selection signal, the selection signal activating one of the plurality of memory areas to create an activated memory area containing a first programm code representing a first device configuration, and deactivating the one of the remaining memory areas to create a deactivated memory area for storing a second programm code representing a second device configuration.

Prefered embodiments and developments of the object of the invention are defined by the respective subclaims.

Further, the invention consists in a method for programming a field mounted device running a computational process, the method comprising the steps of:

activating a first memory area storing a first programmable configuration;

deactivating a second memory area storing a second programmable configuration;

configuring the second memory area with a modification of the second programmable configuration; and

coordinating the configuration of the second memory area with the computational process, the coordination of the configuration of the second memory area including the steps of simultaneously executing the first programmable configuration in the first memory area by the computational process during configuration of the second memory area with a modification of the second programmable configuration, deactivating the first memory area storing the first programmable configuration upon completion of configuring the second memory area with a modification of the second programmable configuration, and activating the second memory area upon completion of configuring the second memory area with a modification of the second programmable configuration.

Prefered embodiments and developments of the method of the invention are defined by the respective subclaims.

One advantage of the invention is that during reconfiguration, the first program code, which represents the current configuration of the field mounted device electronics, can be loaded unchanged, so that the software being executed is always in a consistent state. Since the field mounted device electronics are operational during reconfiguration, the latter can also be carried out while the field mounted device is in operation.

Another advantage of the invention is that the deactivation of the first configuration and the activation of the second configuration take place simultaneously and, even in the event of a failure of the external power supply, can be reliably and consistently completed using the energy

reserves commonly stored in such field mounted devices, particularly in intrinsically safe devices.

The invention and further advantages will become more apparent by reference to the following description of embodiments taken in conjunction with the accompanying drawings. Like reference characters have been used to designate like elements throughout the various figures; where appropriate, reference characters that were already introduced are not repeated in subsequent figures.

Brief description of the Drawings

Fig. 1 is a schematic block diagram of an embodiment of a programmable field mounted device with field mounted device electronics;

Fig. 2 is a schematic block diagram illustrating a preferred embodiment of a method of reconfiguring the field mounted device electronics of Fig. 1;

Fig. 3 is a flowchart showing the steps of the method in accordance with the invention; and

Fig. 4 is a flowchart showing the steps of a development of the method in accordance with the invention.

Detailed description of the Drawings

While the invention is susceptible to various modifications and alternative forms, exemplary embodiments thereof have been shown by way of example in the drawings and will

herein be described in detail. It should be understood, however, that there is no intent to limit the invention to the the particular forms diclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the pirit and scope of the inevntion as defined by the intended claims.

Fig. 1 shows, in block-diagram form, an embodiment of a field mounted device which serves to generate at least one analog or digital measurement signal x_{12} that is representative of a process variable x_{11}, e.g., a tank contents level, a volumetric and/or mass flow rate of a moving fluid, a pressure, or a pH value and/or a temperature of a medium, etc.

To send data, e.g., the measurement signal x_{12}, to other process-monitoring and/or process-controlling information systems, e.g., to a stored-program controller and/or a process control computer, and/or to receive data, e.g., settings, the field mounted device comprises field mounted device electronics 1, which are coupled to an external bus system 2 via a communications interface 11. Such bus systems, e.g., Profibus-PA, Foundation Fieldbus, CANbus, etc., besides transmitting data, also serve to conduct power to the connected field mounted devices.

For communications interface 11, both a two-wire interface, such as the standard interface RS-485 or a 4- to 20-mA current loop, and a multiwire interface, such as the standard interfaces RS-422, TTY, etc., as well as the corresponding communications protocols can be used.

Depending on the design of communications interface 11, the field mounted device is connectable to bus system 2 either directly or via remote I/O modules. In the latter case, use can be made of a smart protocol, such as HART, INTENSOR, etc., in which analog measurement signal x_{12} is frequency- or amplitude-modulated to transmit digital data.

According to a preferred development of the invention, a sensor 3, which responds to process variable x_{11}, is connected to the field mounted device. Sensor 3 converts process variable x_{11} into a sensor signal x_{31} representing the process variable, particularly into an analog signal, such as a signal current, a signal voltage, or a frequency signal. Sensor 3 may be, for example, a Coriolis mass flow rate sensor, an electromagnetic volumetric flow sensor, a pressure transmitter, a pH electrode arrangement, a temperature sensor, a level sensor, etc.

As shown in Fig. 1, sensor signal x_{31} from sensor 3 is applied to the input of a converter circuit 13 of field mounted device electronics 1, which converter circuit 13 serves to convert the signal to a digital sensor signal x_{32}. To accomplish this, sensor signal x_{31} may be passed through an antialiasing filter, sampled, held, and digitized using suitable A/D converters. The digital sensor signal x_{32} is applied from the output of converter circuit 13 via an addressable signal port to a data bus of an internal bus system 12 of field mounted device electronics 1. In addition to or in place of sensor 3, which is connected via converter circuit 13 to internal bus system 12, a further field mounted device, particularly a measured-data-transmitting device, may, of course, be

connected to internal bus system 12 via a suitable interface.

Besides digitizing the sensor signal x_{31}, field mounted device electronics 1 serve to convert digital sensor signal x_{32} to measurement signal x_{12} and to generate communications protocols. Furthermore, field mounted device electronics 1 may provide drive signals to sensor 3, particularly signals serving to excite the sensor electrically or electromechanically.

Field mounted device electronics 1 are preferably contained in a single electronics housing of the field mounted device; in the case of modular field mounted devices with a sensor module and a 10 signal processing module, for example, the measuring electronics may also be distributed between the two modules.

Field mounted device electronics 1 can be implemented, for example, using conventional ASIC and/or SMD technologies.

During the service life of field mounted devices of the kind described, one or more modifications implemented in field mounted device electronics 1, which comprise, for example, recalibrations of field mounted device electronics 1, improvements in implemented evaluation procedures, and/or modifications to communications protocols, are generally initiated on the part of the user and/or on the part of the manufacturer.

In present-day field mounted devices, therefore, such signal processing routines, for which modifications are to

be expected, are commonly stored persistently as fixed-programmed software. "Persistent" means that the software can, on the one hand, be read and thus executed even after a restart of field mounted device electronics 1, particularly after a power fail restart, and, on the other hand, be reprogrammed, particularly to reconfigure field mounted device electronics 1.

As shown in Fig. 1, field mounted device electronics 1 therefore comprise a control circuit 14 with at least one microprocessor 141, which has access, preferably via bus system 12, to digital sensor signal x_{32} and to software persistently stored in a nonvolatile data memory circuit 15 of field mounted device electronics 1. Furthermore, external processes that communicate with field mounted device electronics 1 via bus system 2 have write and/or read access to data memory circuit 15, and thus to the stored software.

Data memory circuit 15 can be implemented, for example, with one or more EEPROM circuits. It is also possible, of course, to implement data memory circuit 15 using other nonvolatile memory circuits familiar to those skilled in the art, such as flash EEPROM, EPROM, and/or CMOS circuits.

For the implementation of fast signal processing routines, particularly of routines that are executed in real time, field mounted device electronics 1 preferably comprise a fast-access volatile data memory circuit 16 serving as a main memory, into which program codes to be frequently executed can be loaded, for example from data memory circuit 15. Data memory circuit 16 may, for instance, be

coupled to control circuit 14 via internal bus system 12 and/or be incorporated as a cache memory in control circuit 14. Data memory circuit 16 can be implemented with static and/or dynamic RAM circuits, for example.

Field mounted device electronics 1 further comprise energy storage electronics 17, e.g. an energy-storing accumulator and/or a capacitance network, which preferably serve to store energy required for at least one write access to data memory circuit 15, particularly also during a failure of the power supply via bus system 2.

As shown in Fig. 2, the software stored in data memory circuit 15 comprises at least a first program code C_{151}, which represents a first configuration of field mounted device electronics 1 and occupies an activated first memory area 151 of data memory circuit 15. "Activated memory area" means that at least one computational process tskl running in microprocessor 141 has read access to this memory area and can execute the stored program code, e.g., program code C_{151} correspondingly, "deactivated memory area" means that at this moment no computational process running in microprocessor 141 has read or write access to this memory area.

To reconfigure field mounted device electronics 1, according to an advantageous feature of the invention, program code C_{151} is replaced by a second program code C_{152}, which serves to reprogram the implemented software and represents a second configuration of field mounted device electronics 1, such that the second program code C_{152}, as symbolized in Fig. 2 by a dash-dot arrow, is executable or

executed by computational process tsk1 instead of program code C_{151}. As shown in Fig. 1, to modify the software being executed, data memory circuit 15 further comprises at least one activatable second memory area 152, which contains program code C_{152}. The program codes can be complete programs, such as signal processing routines generating measurement signal x_{12}, individual program steps, and/or calibration data for the field mounted device that are coded as program parameters.

Furthermore, routines for implementing communications interfaces and/or for driving peripheral indicating and control elements may be stored as program codes in data memory circuit 15. Program codes of the kind described can be generated and implemented in data memory circuit 15 both by the manufacturer and by the user, particularly during or after start-up of the field mounted device.

As shown in Fig. 3, during operation of field mounted device electronics 1, computational process tsk1 has read access to memory area 151 during a time interval represented as step 100. In this step 100, program code C_{151} is thus executed, at least temporarily, in computational process tsk1. To create program code C_{152} in a further step 200, a first configuration process tsk2 is started, which sends corresponding modification data TD, e.g., manually entered data, to data memory circuit 15. To that end, configuration process tsk2 preferably has both write and read access to data memory circuit 15.

Configuration process tsk2 may be, for example, an editor program running in field mounted device electronics 1 or in

an external programming device connected to communications interface 11 via the above-mentioned modem, or a routine that loads the modification data TD from a mass storage into data memory circuit 15. Configuration process tsk2 may also run on an external programming device that sends the modification data TD via bus system 2.

One advantage of the invention is that the field mounted device can remain in the measurement mode during the reconfiguration of field mounted device electronics 1, i.e., even during reconfiguration, executable software is always contained in data memory 15. To that end, as shown in Fig. 3, memory area 151 is active even after the starting of configuration process tsk2, so that at least the aforementioned computational process tsk1 can still execute program code C_{151}, which represents the currently valid first configuration.

In such a multiuser environment comprising computational process tsk1 and configuration process tsk2, read and/or write accesses to data memory circuit 15 must be coordinated so that executable software, particularly software conforming to the predetermined measurement tasks, is activated at all times; accordingly, modifications that may result in inconsistencies of the executed software with respect to the measurement tasks must be prevented. To accomplish this, in step 400, a coordination process tsk4 is started in control circuit 14. This coordination process tsk4 controls the read and/or write access to data memory circuit 15 by processes running in microprocessor 141, particularly by configuration process tsk2 and/or by computational process tsk1.

Coordination process tsk4 may be performed, for example, by a persistency manager of a database implemented in field mounted device electronics 1. The persistency manager may be controlled by a higher-level transaction manager of the database. This database is also persistently stored as software in data memory circuit 15. For the execution of this software, the persistency manager and, if present, the transaction manager may also be loaded into data memory circuit 16.

After the start of configuration process tsk2, in step 401, this process is registered in coordination process tsk4, which is being executed in control circuit 14.

Coordination process tsk4 then reserves the currently deactivated memory area 152 for configuration process tsk2, such that in step 201, configuration process tsk2 is granted exclusive write access to memory area 152. Thus, any configuration processes running parallel with configuration process tsk2 cannot write data into memory area 152.

This is followed by the aforementioned sending of modification data TD by configuration process tsk2 to data memory circuit 15, which is represented as step 202. After program code C_{152} has been transferred completely, particularly error-free, by configuration process tsk2 into memory area 152, in step 203, configuration process tsk2 sends an end-of-transmission characterizing command EOT to coordination process tsk4.

To reconfigure field mounted device electronics 1, it is now only necessary to activate memory area 152 with program code C_{152}. Since only one configuration of field mounted device electronics 1 may be valid at a time, i.e., since only one of memory areas 151, 152 may be activated at the same time, the activated memory area 151 must first be deactivated.

As shown in Fig. 3, the deactivation of memory area 151 and the activation of memory area 152 are carried out in a single step 500, which is also controlled by coordination process tsk4. A digital selection signal x_{14} for deactivating memory area 151 and activating memory area 152 is generated by control circuit 14. Selection signal x_{14} may be, for example, a write instruction addressed and sent to data memory circuit 15 and serving to replace a persistently stored first branch address, which refers to memory area 151, by a second branch address, which refers to memory area 152; furthermore, the write instruction serving as the selection signal x_{14} may cause a coded identification of the first branch address, which controls the computational process, to be replaced by a coded identification of the second branch address.

Since memory areas 151, 152 are practically operated as exchange buffers, field mounted device electronics 1 are in a critical state for only a short duration, namely for the time of switching from activated memory area 151 to activated memory area 152, during which the first configuration is out of operation and the second configuration is not yet in operation. The switching of memory areas 151, 152 is accomplished by a single write

access to data memory circuit 15 and can be readily buffered, using in particular the energy reserves stored in energy storage circuit 17. Thus, during reconfiguration and/or after a failure of the above-mentioned external power supply, the currently valid software, and hence field mounted device electronics 1, is always in an executable condition.

After completion of step 500, computational process tskl, as shown schematically in Fig. 3 as step 101, can execute program code C_{152} which is contained in memory area 152. The activated program code C_{151} may, of course, be replaced by another program code in the manner described above.

According to another preferred development of the method of the invention, prior to the starting of configuration process tsk2, program code C_{151}, which is contained in memory area 151, is transferred into memory area 152 by read/write operations controlled by microprocessor 141, so that a backup copy of program code C_{151} is retained. Thus, program code C_{151} is available with a high degree of probability even in the event of a software and/or hardware error in memory area 151, and can be reactivated in a simple manner using, for example, a further selection signal that activates memory area 152. The copying of program code C_{151} can be done immediately after the loading of program code C_{151} or after activation of memory area 151, for example. In an analogous manner, program code C_{152} can be copied from memory area 152 to memory area 151 after deactivation of memory area 151.

Data memory circuit 15 can advantageously be implemented as a monolithic circuit comprising memory area 151, 152. Memory area 151 and/or memory area 152 can also be implemented as modules that are permanently or nonpermanently coupled to bus system 12, the nonpermanent connection being preferably a plug-in connection. In that case, activated memory area 152 may also be implemented with an external memory circuit, e.g., a data memory circuit in the aforementioned programming device connected to field mounted device electronics 1, to which field mounted device electronics 1 have at least temporary read access.

According to a further preferred development of the field mounted device of the invention, data memory circuit 15 further comprises a temporarily activatable third memory area 153 for storing a third program code C_{153} which represents a third configuration of the field mounted device.

According to a further preferred development of the method of the invention, after registration of configuration process tsk2 in coordination process tsk4, a second configuration process tsk3 is started such that the two configuration processes tsk2, tsk3 run in parallel, i.e., practically simultaneously, as represented in Fig. 4 by a step 300. Then, in a step 402, configuration process tsk3 is also registered in coordination process tsk4, and in a step 301, currently deactivated memory area 153 is reserved for configuration process tsk3. The reserving of memory area 153 is done analogously to the reserving of memory area 152 that configuration process tsk3 has exclusive

write access to memory area 153. By means of coordination process tsk4, memory area 153 is simultaneously adjusted so that computational processes such as computational process tskl have neither read nor write access to it.

Furthermore, configuration process tsk2 cannot write data into memory area 153, either.

According to a further preferred development of the s method of the invention, after registration of configuration process tsk2, memory area 152 is adjusted by coordination process tsk4 so that configuration process tsk3 has read access to memory area 152. Thus, the modifications made to the software in memory area 152 by configuration process tsk2 can be followed by configuration process tsk3 and be taken into account in the creation of program code C_{153}.

While the invention has been illustrated and described in detail in the drawings and forgoing description, such illustration and description is to be considered as exemplary not restrictive in character, it being understood that only exemplary embodiments have been shown and described and that all changes and modifications that come within the spirit and scope of the invention as described herein are desired to protected.

What is claimed is:

1. A method for programming a field mounted device having a memory, the method comprising the steps of:

running a computational process having data read access to an activated first memory area storing a programmable first device configuration;

deactivating the first memory area, wherein said step comprises precluding said computational process to access the first memory area; and

activating a deactivated second memory area storing a programmable second device configuration, wherein said step comprises granting said computational process data read access to the second memory area.

2. The method of claim 1, further comprising the steps of:

running a first configuration process having data read and write access to the deactivated second memory area; and

storing data in the second memory area for modifying the second device configuration in the second memory area.

3. The method of claim 2, further comprising the step of

executing the first device configuration in the first memory area by the computational process during running the first configuration process.

4. The method of claim 2, further comprising the steps of:

running a second configuration process having data read and write access to a deactivated third memory area; and

storing data in the third memory area.

5. The method of claim 3, further comprising the steps of:

precluding the second configuration process access to the second memory area by granting the first configuration process an exclusive access to the second memory area;

modifying via said second configuration process the second device configuration in the second memory area; and

granting the computational process access to the second memory area after said modifying step.

6. The method of claim 2, further comprising the step of

storing the first device configuration into the second memory area.

7. The method of claim 1, further comprising the steps of:

writing over a first branch address that references the first memory area with a second branch address that references the second memory area for deactivating the first memory area and activating the second memory area in a single write access.

8. The method of claim 7, further comprising the steps of:

deactivating the first memory area upon the occurrence of a hardware or software error in the first memory area; and

activating the second memory area upon said occurrence of said error.

9. The method of claim 7, further comprising the step of

copying the first device configuration from the first memory area into the second memory area.

10. The method of claim 9, further comprising the step of

executing the first device configuration in the first memory area by the computational process during the copying step.

11. A programmable field mounted device, comprising:

a memory circuit including a plurality of memory areas, each memory area storing program codes, each memory area selectively activated;

a control circuit configured to generate a selection signal, the selection signal activating one of the plurality of memory areas to create an activated memory area containing a first programm code representing a first device configuration, and deactivating the one of the remaining memory areas to create a deactivated memory area for storing a second programm code representing a second device configuration.

12. The device of claim 11, wherein the control circuit includes a microprocessor, the microprocessor having read access to the activated memory area for excuting the first programm code.

13. The device of claim 11, further comprising a configuration device configured to modify the second program code in the deactivated memory area.

14. The device of claim 13, wherein the control circuit is configured to grant the configuration device read and write access to the deactivated memory area for modifying the second programm code.

15. The device of claim 11, wherein the control circuit is further configured to deactivate the activated memory area containing the first program code and activate the deactivated memory area containing the modified second program code.

16. The device of claim 12 and 15, wherein the control circuit is further configured to provide the microprocessor read access to the memory area containing the second programm code for executing said program code.

17. The device of claim 11, wherein the deactivated memory area containing the second programm code is activated by

writing in the memory circuit a branch address corresponding to said memory area.

18. The device of claim 11, wherein the activated memory area containing the first programm code is deactivated by writing over a branch address in the memory circuit corresponding to said memory area address with the branch address corresponding to the memory area containing the second programm code.

19. The device of claim 11, wherein the memory circuit is a non-volatile memory.

20. The device of claim 11, wherein the memory circuit is an EEPROM.

21. The device of claim 11, further including an energy storage device configured to store energy for at least one write access to the memory circuit.

22. A method for programming a field mounted device running a computational process, the method comprising the steps of:

activating a first memory area storing a first programmable configuration;

deactivating a second memory area storing a second programmable configuration;

configuring the second memory area with a modification of the second programmable configuration; and

coordinating the configuration of the second memory area with the computational process, the coordination of the configuration of the second memory area including the steps of simultaneously executing the first programmable configuration in the first memory area by the computational process during configuration of the second memory area with a modification of the second programmable configuration, deactivating the first memory area storing the first programmable configuration upon completion of configuring the second memory area with a modification of the second programmable configuration, and activating the second memory area upon completion of configuring the second memory area with a modification of the second programmable configuration.

23. The method of claim 22, wherein the step of

activating the second memory area and deactivating the first memory area comprises the step of writing over a first branch address that references the first memory with a second branch address that references the second memory area.

24. The method of claim 22, wherein the step of coordinating the configuration of the second memory area with the computational process further comprises the steps of:

precluding the computational process access to the second memory area;

granting a configuration process exclusive access to the second memory area; and

granting the computation process access to the second memory area after the modifying step.

25. The method of claim 22, wherein the step of activating the second memory area and deactivating the first memory area is accomplished by a single write access to a branch address.

Abstract

Programmable Field Mounted Device

To programming the device during running a computational process in device electronics, the device having a activated first memory area storing a first programmable configuration and a deactivated second memory area storing a second programmable configuration. The the second programmable configuration is modified. Simultaneously, the first programmable configuration in the first memory area is executed by the computational process. Upon completion of configuring the second memory area, the first memory area is deactivated and the second memory area is activated for excecuting by the computational process.

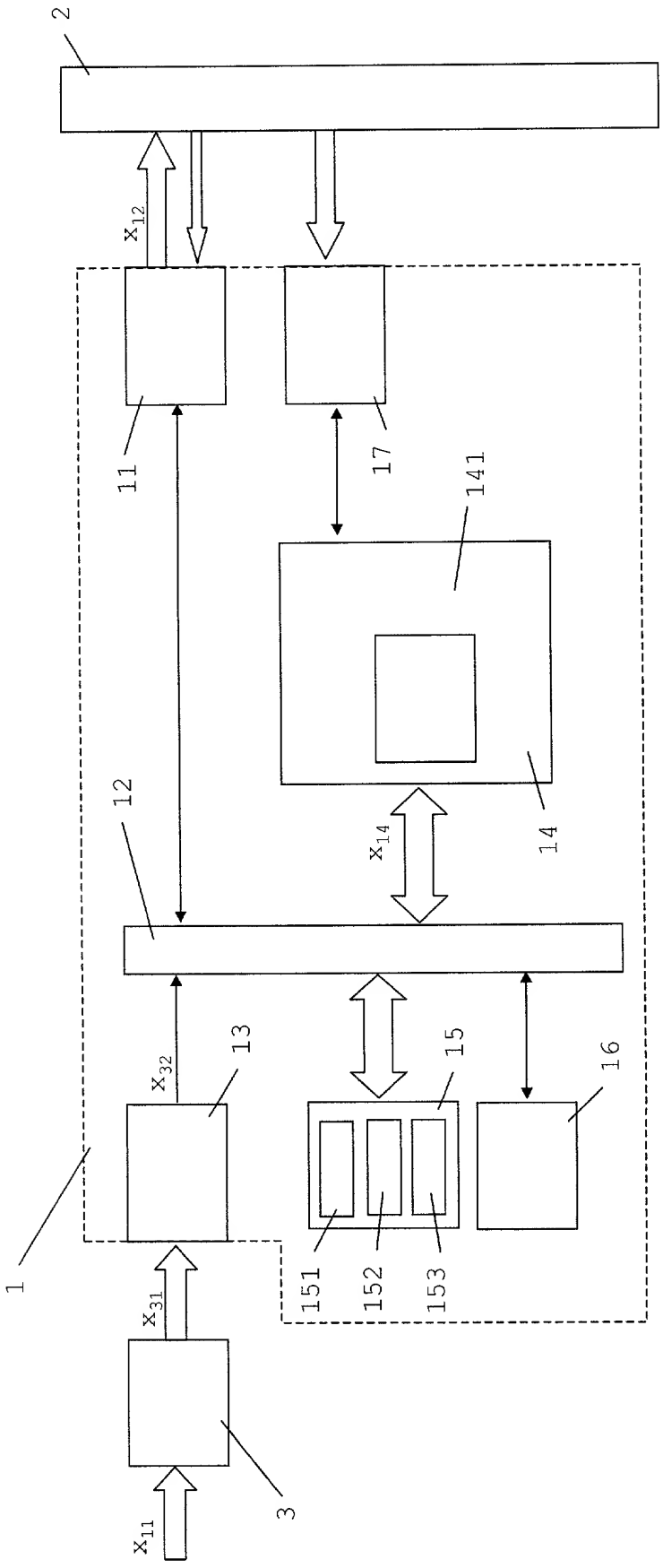

Fig. 1

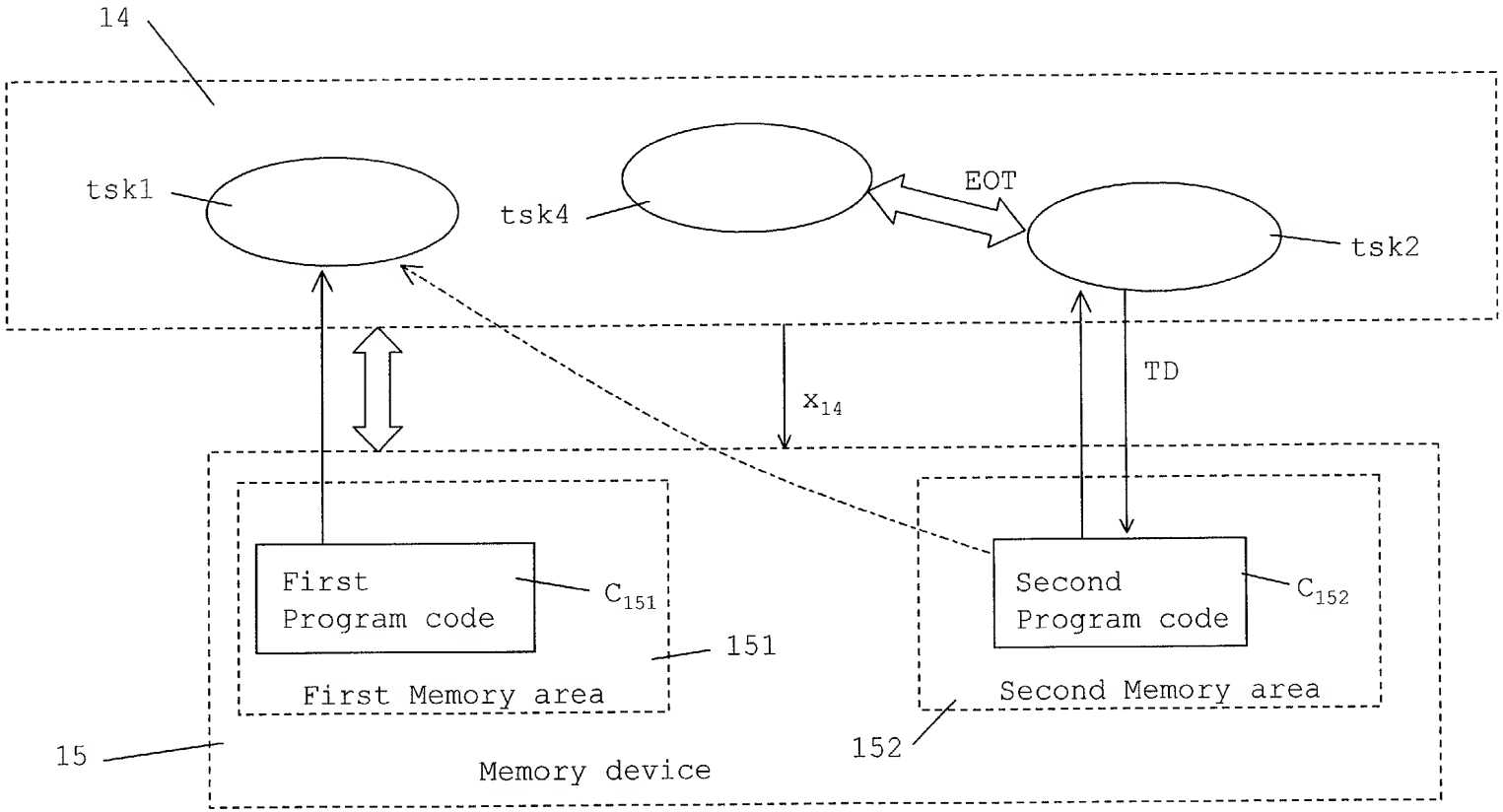
14
tsk1
tsk4
EOT
tsk2
x_{14}
TD
First
Program code
C_{151}
151
First Memory area
Second
Program code
C_{152}
Second Memory area
15
Memory device
152

Fig. 2

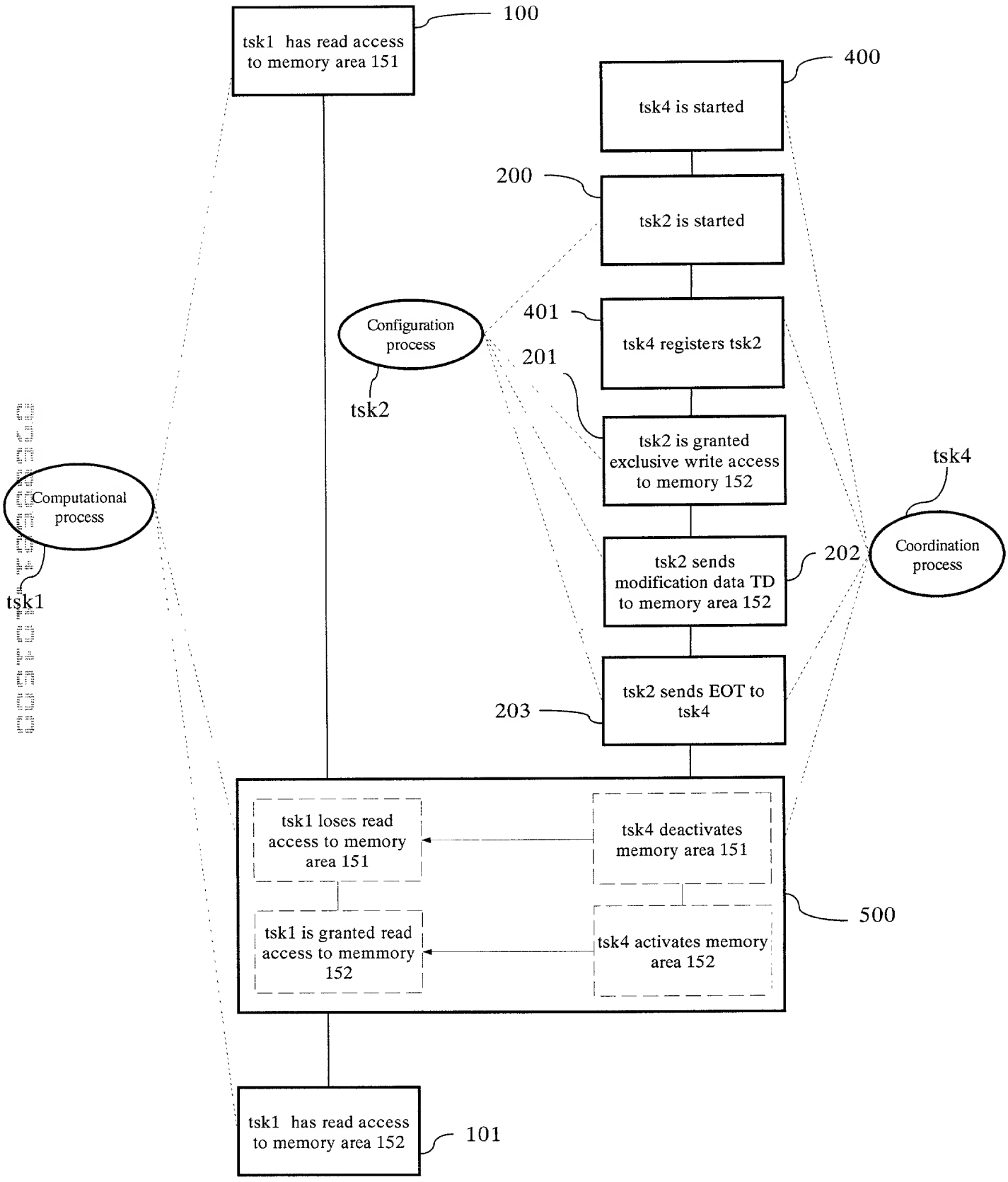
tsk1 has read access to memory area 151
100
tsk4 is started
400
200
tsk2 is started
Configuration process
tsk2
401
tsk4 registers tsk2
201
tsk2 is granted exclusive write access to memory 152
tsk4
Computational process
tsk1
tsk2 sends modification data TD to memory area 152
202
Coordination process
tsk2 sends EOT to tsk4
203
tsk1 loses read access to memory area 151
tsk4 deactivates memory area 151
tsk1 is granted read access to memmory 152
tsk4 activates memory area 152
500
tsk1 has read access to memory area 152
101

Fig. 3

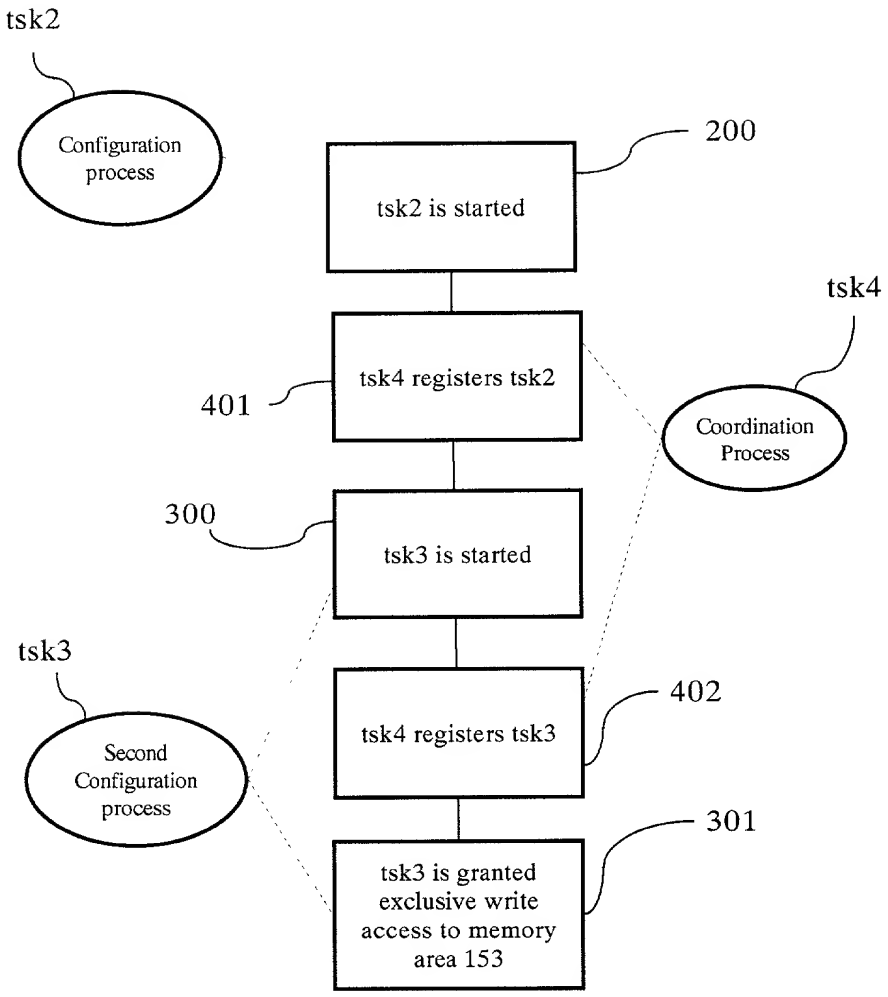
tsk2
Configuration process
200
tsk2 is started
tsk4
401
tsk4 registers tsk2
Coordination Process
300
tsk3 is started
tsk3
Second Configuration process
402
tsk4 registers tsk3
301
tsk3 is granted exclusive write access to memory area 153

Fig. 4

Attorney Docket No.: FL0118-US

DECLARATION AND POWER OF ATTORNEY -- PATENT APPLICATION

As below named inventor, I hereby declare that I believe I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter which is claimed and for which a patent is sought in the application entitled:

PROGRAMMABLE FIELD DEVICE

the specification of which

(check one) _x_ is attached hereto
___ ___was filed on _____ as
United States Application Serial No. _____ or
PCT International Application No. _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to herein.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 1 19(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
99 12 0713.5	European Patent Office	Oct. 18, 1999	☐	☐	☒
00 10 2813.3	European Patent Office	Feb. 11, 2000	☐	☐	☒
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/204,993	May 16, 2000	☐ Additional provisional application numbers are listed on a supplemental priority data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(If applicable)*

☐ **Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet attached hereto.**

As a named inventor, I hereby appoint James A. Coles, Reg. No. 28,291; E. Victor Indiano, Reg. No. 30, 143; Ronald K. Aust, Reg. No. 36,735; and Anthony P. Filomena, Reg. No. 44,108; as attorneys of record, and William S. Meyers, Reg. No. 42,884; as agent of record, with full power of substitution and revocation, to prosecute this application, and to transact all business in the Patent and Trademark Office connected therewith, and I specify that communications regarding the application be directed to:

Intellectual Property Group
Bose McKinney & Evans LLP
135 North Pennsylvania Street, Suite 2700
Indianapolis, Indiana 46204
Telephone: (317) 684-5000
Facsimile: (317) 684-5173

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Jochen STINUS
Full Name of Sole or First Joint Inventor

Jochen Stinus
Inventor's signature

Germany
Country of Citizenship

Sept. 25, 2000
Date

Bützmattweg 45

D-79594 Inzlingen, GERMANY
Residence and Post Office Address

Monika BANZHAF
Full Name of Second Joint Inventor

Monika Banzhaf
Inventor's signature

Germany
Country of Citizenship

Sept. 20, 2000
Date

Im Pfädlen 1

D-70439 Stuttgart, GERMANY
Residence and Post Office Address

Full Name of Third Joint Inventor

Inventor's signature

Country of Citizenship

Date

Residence and Post Office Address